EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	406	716/14.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 12:15
S18 3	527	716/13.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:51
S18 2	28	716/12.ccls. and layer and (filler dummy spacer) same cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:50
S18 1	898	716/12.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:28
S17 9	281	716/9.ccls. and (filler spacer dummy feed-through through) and cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:19
S18 0	35	716/9.ccls. and (filler spacer dummy feed-through) and cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:04
S17 8	35	716/9.ccls. and (filler spacer dummy) and cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:03
S17 7	445	716/9.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 11:01

EAST Search History

S176	1511	716/10-11.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 21:50
S174	109	metal same layer same power same wir$3 and (toshiba ricoh) and (interconnect$3 connect$3 intra adj 2connect$3) and (power ground) near4 (line wir$3 rail) and signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 21:47
S173	167	metal same layer same power same wir$3 and (toshiba ricoh) and (interconnect$3 connect$3 intra adj 2connect$3) and (power ground) near4 (line wir$3 rail)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 21:31
S171	18	metal same layer same power same wir$3 and ricoh	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 21:29
S170	8	((through filler) adj3 cell spacer) and structur$2 and metal and multi adj2 layer and (ground power) near4 (rail wir$3 line) and (interconnect$3 connect$3) and signal and region and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:56
S169	205	((through filler) adj3 cell spacer) and structur$2 and metal and multi adj2 layer and (ground power) near4 (rail wir$3) and (interconnect$3 connect$3) and signal and region	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:30
S168	205	((through filler) adj3 cell spacer) and structure and metal and multi adj2 layer and (ground power) near4 (rail wir$3) and (interconnect$3 connect$3) and signal and region	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:30
S167	7	((through filler) adj3 cell spacer) and structure and metal and multi adj2 layer and (ground power) near4 (rail wir$3) and (interconnect$3 connect$3) and signal and region and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:29

EAST Search History

S166	32	((through filler) adj3 cell) and structure and metal and layer and (ground power) near4 (rail wir$3) and (interconnect$3 connect$3) and signal and region and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:26
S165	187	((through filler) adj3 cell) and structure and metal and layer and (ground power) near4 (rail wir$3) and interconnect$3 and signal and region	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:10
S163	293	((through filler) adj3 cell) and structure and metal and layer and (ground power) near4 (rail wir$3) and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:09
S161	3	filler adj cell same structure and metal and layer and (ground power) near4 (rail wir$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 20:07
S160	2	filler adj cell same structure and metal and layer and (ground power) adj (rail wir$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:55
S159	30	filler adj cell same structure and metal and layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:55
S158	2	(multi adj2 layer) same interconnect$3 same metal and (filler dummy through) adj4 cell and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:54
S157	55	(multi adj2 layer) same interconnect$3 same metal and (filler dummy through) adj4 cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:34

EAST Search History

S156	1885	(multi adj2 layer) same interconnect$3 same metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:32
S154	24	filler adj cell same layer and metal and (interconnect$3 connect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:57
S153	27	filler adj cell same layer and metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:57
S152	50	filler adj cell same layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:56
S151	30	(non adj2 used) same (through same cell) same (metal layer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:56
S150	1	(non adj used) adj4 (through adj2 cell) same (metal layer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:54
S149	9	S147 and S148	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:22
S148	8370	signal adj (line wir$3) same distan$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:05

EAST Search History

S147	1662	S146 and S141	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:04
S146	33025	(filler feed adj2 through dummy adj cell) same (upper lower) same (layer metal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:03
S140	3145	(filler adj cell feed adj2 through dummy adj cell) same (upper lower) same (layer metal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:03
S145	1	S140 and S141 and signal and via and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:01
S144	73	S140 and S141 and signal and via	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:01
S143	137	S140 and S141 and signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:01
S142	383	S140 and S141	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:00
S141	327583	(connect$3 interconnect$3 inter-connect$3) same (power ground) same (rail wir$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 17:59

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S131	9	S127 and S128 and S129 and S130	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/15 12:22
S130	479964	signal adj3 (line wir$3 path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/15 10:57
S129	34386	(upper lower) adj4 (layer metal) same (power ground vdd vss supply)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/15 10:55
S128	79099	(multi$3 plurality more) adj4 (layer) same metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/15 10:53
S127	14942	(filler dummy feed-through) with cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/15 10:50

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	778	716/11.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 17:04
L3	936	716/10.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/17 16:07

Terms used **filler cell layer metal**

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1 HAPPI: a chip compiler based on double-level-metal technology

Rathin Putatunda, David Smith, Stephen McNeary, James Crabbe

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(853.27 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a unique fully automatic chip compiler, HAPPI, that uses double-level-metal technology and 3 levels of interconnection to realize high-speed and maximum-density chip designs consisting of a varying mixture of custom and standard-cell macros within a chip topology that guarantees 100% signal and power routing. A heuristic technique for generating placements of "soft macros" that are balanced in both area and connectivity has been presented. A routing approach ...

2 An advanced multichip module (MCM) for high-performance UNIX servers

J. U. Knickerbocker, F. L. Pompeo, A. F. Tai, D. L. Thomas, R. D. Weekly, M. G. Nealon, H. C. Hamel, A. Haridass, J. N. Humenik, R. A. Shelleman, S. N. Reddy, K. M. Prettyman, B. V. Fasano, S. K. Ray, T. E. Lombardi, K. C. Marston, P. A. Coico, P. J. Brofman, L. S. Goldmann, D. L. Edwards, J. A. Zitz, S. Iruvanti, S. L. Shinde, H. P. Longworth

November 2002 **IBM Journal of Research and Development**, Volume 46 Issue 6

Publisher: IBM Corp.

Additional Information: full citation, abstract, references, citings

In 2001, IBM delivered to the marketplace a high-performance UNIXÂ®-class eServer based on a four-chip multichip module (MCM) code named Regatta. This MCM supports four POWER4 chips, each with 170 million transistors, which utilize the IBM advanced copper back-end interconnect technology. Each chip is attached to the MCM through 7018 flip-chip solder connections. The MCM, fabricated using the IBM high-performance glass-ceramic technology, features 1.7 million internal copper vias and high-den ...

3 On Whitespace and Stability in Mixed-Size Placement and Physical Synthesis

Saurabh N. Adya, Igor L. Markov, Paul G. Villarrubia

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(1.73 MB) Additional Information: full citation, abstract, index terms

In the context of physical synthesis, large-scale standard-cell placementalgorithms must facilitate incremental changes to layout, bothlocal and global. In particular, flexible gate sizing, net buffering anddetail placement require a certain amount of unused space in everyregion of the die. The need for "local" whitespace is further emphasizedby temperature and power-density limits. Another requirement,the stability of placement

Fri, 17 Feb 2006, 10:29:08 AM EST

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#2 ((filler<in>metadata) <and> (cell <in>metadata))<and> (multilayer<in>metadata)

#3 ((filler cell<in>metadata) <and> (metal<in>metadata))<and> (interconnect<in>metadata)

#4 (dummy cell<in>metadata)

#5 ((filler cell<in>metadata) <and> (metal<in>metadata))<and> (multilayer<in>metadata)

#6 ((dummy cell<in>metadata) <and> (metal<in>metadata)) <and> (layer<in>metadata)

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((filler <in>metadata) <and> (cell<in>metadata)) Search

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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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☐ 1. **Cell radius & guard band requirements by mutual interference investigati satellite digital multimedia broadcasting systems using gap-filler**
In Suk Cha; Sung Ho Park; KyungHi Chang;
Vehicular Technology Conference, 2005. VTC 2005-Spring. 2005 IEEE 61st
Volume 4, 30 May-1 June 2005 Page(s):2638 - 2642 Vol. 4
Digital Object Identifier 10.1109/VETECS.2005.1543813
AbstractPlus | Full Text: PDF(4912 KB) IEEE CNF
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☐ 2. **AMTEC recirculating test cell component testing and operation**
Underwood, M.L.; Sievers, R.K.; O'Connor, D.; Williams, R.M.; Jeffries-Nakam C.P.;
Energy Conversion Engineering Conference, 1989. IECEC-89. Proceedings of Intersociety
6-11 Aug. 1989 Page(s):2833 - 2839 vol.6
Digital Object Identifier 10.1109/IECEC.1989.74395
AbstractPlus | Full Text: PDF(872 KB) IEEE CNF
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☐ 3. **Hybrid type bipolar plate for proton exchange membrane fuel cell**
Junbom Kim; Youngmo Goo; Seungeul Yoo;
Science and Technology, 2005. KORUS 2005. Proceedings. The 9th Russian-International Symposium on
26 June-2 July 2005 Page(s):462 - 465
Digital Object Identifier 10.1109/KORUS.2005.1507758
AbstractPlus | Full Text: PDF(264 KB) IEEE CNF
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☐ 4. **A satellite based ATM switch**
Chellingsworth, S.P.;
Networking Aspects of Small Terminal Satellite Systems, IEE Colloquium on
17 Nov 1994 Page(s):9/1 - 9/6
AbstractPlus | Full Text: PDF(360 KB) IEE CNF

☐ 5. **Designing lithium ion batteries for high power applications**
Ismail, M.; Hassan, M.F.; Winnie, T.; Arof, A.K.; Nor, K.M.;
Power Engineering Conference, 2003. PECon 2003. Proceedings. National
15-16 Dec. 2003 Page(s):289 - 291
Digital Object Identifier 10.1109/PECON.2003.1437459
AbstractPlus | Full Text: PDF(821 KB) IEEE CNF
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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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☐ 1. **Radiation hardening of dynamic memories by the use of a new dummy ce**
Schleifer, H.; v.d. Ropp, T.; Reczek, W.;
Memory Technology, Design and Testing, 1994., Records of the IEEE Internat on
8-9 Aug. 1994 Page(s):126 - 129
Digital Object Identifier 10.1109/MTDT.1994.397186
AbstractPlus | Full Text: PDF(192 KB) IEEE CNF
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☐ 2. **Design concept for radiation hardening of low power and low voltage dyr**
Schleifer, H.; Ropp, T.v.d.; Hoffmann, K.; Reczek, W.;
Solid-State Circuits, IEEE Journal of
Volume 30, Issue 7, July 1995 Page(s):826 - 829
Digital Object Identifier 10.1109/4.391125
AbstractPlus | Full Text: PDF(288 KB) IEEE JNL
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☐ 3. **A 60-ns 16-Mbit DRAM with a minimized sensing delay caused by bit-line capacitance**
Chou, S.; Takano, T.; Kita, A.; Ichikawa, F.; Uesugi, M.;
Solid-State Circuits, IEEE Journal of
Volume 24, Issue 5, Oct 1989 Page(s):1176 - 1183
Digital Object Identifier 10.1109/JSSC.1989.572575
AbstractPlus | Full Text: PDF(804 KB) IEEE JNL
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☐ 4. **A general-purpose two-dimensional process simulator-OPUS for arbitrar**
Nishi, K.; Sakamoto, K.; Kuroda, S.; Ueda, J.; Miyoshi, T.; Ushio, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 8, Issue 1, Jan. 1989 Page(s):23 - 32
Digital Object Identifier 10.1109/43.21815
AbstractPlus | Full Text: PDF(884 KB) IEEE JNL
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☐ 5. **A 16-Mb CMOS SRAM with a 2.3-μm^2 single-bit-line memory cell**
Sasaki, K.; Ueda, K.; Takasugi, K.; Toyoshima, H.; Ishibashi, K.; Yamanaka, T Ohki, N.;
Solid-State Circuits, IEEE Journal of
Volume 28, Issue 11, Nov. 1993 Page(s):1125 - 1130
Digital Object Identifier 10.1109/4.245592

Results for "((dummy cell<in>metadata) <and> (metal<in>metadata))<and> (layer<i..." e-mail
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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **A 76-mm^2 8-Mb chain ferroelectric memory**
Takashima, D.; Takeuchi, Y.; Miyakawa, T.; Itoh, Y.; Ogiwara, R.; Kamoshida, Doumae, S.M.; Ozaki, T.; Kanaya, H.; Yamakawa, K.; Kunishima, I.; Oowaki, Y
Solid-State Circuits, IEEE Journal of
Volume 36, Issue 11, Nov. 2001 Page(s):1713 - 1720
Digital Object Identifier 10.1109/4.962293
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